METHOD OF MANUFACTURING AN INTEGRATED SEMICONDUCTOR DEVICE HAVING A PLURALITY OF CONNECTION LEVELS

CROSS-REFERENCE TO RELATED APPLICATION

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BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to an integrated semiconductor device having a plurality of connection levels, and a manufacturing method thereof.

Description of the Related Art

As known, the integration of semiconductor devices is always and always increasing, because of the progresses in the semiconductor technology. In particular, the availability of a plurality of metal layers for interconnections has been decisive in making the signal routing more compact.

In devices having a plurality of connection levels (layers of metal or another conductive material), electrical connections exist between connection regions formed in successive connection levels, and between connection levels formed in the first connection level and regions integrated in the device substrate; these connections are formed by through regions (plugs or contacts) extending through the insulating material separating the various connection levels from one another, and from the integrated regions of the device. In addition, connections are sometimes present between connection regions belonging to non-consecutive connection levels, for example between an (N-1)-th metal layer and an (N+1)-th metal layer, or between integrated regions and connection regions that do not

belong to the first metal level. In this case, now, it is necessary to form intermediate regions or islands in the intermediate connection layer (for example the N-th metal layer).

An example of connection between a connection region formed in the third level (third metal layer) and a connection region formed in the first level (first metal layer) is shown in Figures 1a and 1b, which show respectively a top plan view and a cross-section of a device 1. The device 1 comprises a substrate 3 of a first conductivity type (for example P), accommodating an integrated region 4 of a second conductivity type (for example N). On substrate 1 there extend in succession a first dielectric layer 5, a first metal level 6, a second dielectric layer 7, a second metal level 10, a third dielectric layer 9, and a third metal level 11.

The first metal layer 6 comprises a first connection region 6a; the second metal layer 10 comprises second connection regions 10a, and the third metal layer 11 comprises a third connection region 11a. The first connection region 6a is connected to the integrated region 4 by a contact 12, which extends through the first dielectric layer 5; in addition, the first connection region 6a is connected to the third connection region 11a by an intermediate region or "island" 10b, which is formed in the second metal level 10. The intermediate island 10b is connected to the first connection region 6a by a first plug 15 passing through the second dielectric layer 7, and it is connected to the third connection region 11a by a second plug 16 passing through the third dielectric layer 9.

The manufacture of the intermediate island 10b involves a certain bulk, since it is necessary to comply with rules regarding the width of the intermediate island (which is therefore wider than plugs 15, 16), and the minimum distance from the regions (connection regions 10b) formed on the same metal level. It is apparent that when different connections must be provided between connection and/or integrated regions belonging to non-adjacent levels, this results in a considerable spatial dimension. In addition, sometimes, the space required by the intermediate islands does not allow the device layout to be optimized. This is the case for example of non-volatile EPROM, EEPROM and flash-EEPROM memories, wherein it is required to connect all, or a large number, of polysilicon

control gate regions on the first metal level ("word line strap"), and the drain regions on the same bit line on the second metal level to reduce the capacitive connection between the second metal level and the substrate, and thus the parasitic capacities.

SUMMARY OF THE INVENTION

An object of the invention is to provide a solution allowing a reduction in the space necessary for connecting two connection regions, or a connection region and an integrated region of the device, arranged on non-consecutive levels.

According to principles of the present invention, an integrated semiconductor device having a plurality of connections levels and a manufacturing method thereof are provided.

To help understanding of the present invention, preferred embodiments are now described, purely by way of non-limiting example, with reference to the attached drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1A shows a top plan view of a known device.

Figure 1B shows a cross-section through the known device of Figure 1.

Figure 2A shows a top plan view of a device according to the invention.

Figure 2B shows a cross-section through the device of Figure 2A.

Figures 3-8 show cross-sections through a second embodiment relating to a memory device, in successive manufacturing steps.

Figure 9 shows a cross-section through a third embodiment of the invention.

DETAILED DESCRIPTION OF THE INVENTION

In Figures 2A, 2B, the parts of the integrated device 20 in common with the known device 1 of Figures 1A and 1B, are shown with the same reference numbers, and will not be described again.

In detail, in device 20, the intermediate island 10b of the conventional semiconductor device 1 is not present, and a second plug 21 passing through the third dielectric layer 9 extends as far as the first plug 15, and is in direct contact with the latter for connection to the first connection region 6a.

As can be seen, plugs 15, 21 have cross dimensions that are substantially constant and equal to each other. The entire connection structure between the third connection region 11a and the first connection region 6a has a much smaller dimension than the solution of Figure 1B because of the lack of the intermediate island 10b. As already stated, according to the existing integration rules the intermediate island 10b should be much wider than the plugs.

In general, the cross dimensions of plugs 15, 21, and the provided tolerances, are such as to ensure electrical continuity between the plugs 15, 21, even in case of misalignment of the etching masks of the second and third dielectric layers 7, 9. It will be appreciated that the contact area is reduced as the misalignment increases. However, the metal forming the plugs 15, 21 guarantees the electrical continuity. Of course, the dimensions must be designed so that misalignment does not jeopardize the electrical insulation between the plug 21 and the second connection regions 10a. The distance required to guarantee this insulation is however less than the dimensions obtainable photolithographically, such that in any case, elimination of the intermediate islands involves reduction of the dimensions.

To manufacture the device 20, the intermediate island 10b is not formed during shaping of the second metal level 10. Additionally, etching of the third dielectric layer 9 is prolonged such as to additionally remove the dielectric layer to a depth equivalent to the thickness of the second metal level 10, such as to reach the first plug 15. Although etching of the dielectric layer 9 is carried out for a greater thickness than in case of device 1 (Figures 1A, 1B), this will not present a problem because the selectivity of etching between the dielectric material and the metal material is high. Thus, it is possible to prolong etching

without damaging the connection regions where connection apertures are simultaneously formed.

To avoid damaging the lower dielectric layer, in this specific case layer 7, where there is misalignment of the etching masks of the third dielectric layer 9 with respect to the second dielectric layer 7, the second dielectric layer can be formed from two superimposed layers with different etching characteristics. Consequently, the two superimposed layers can be selectively removed. In this case, etching of the third dielectric layer 9 stops automatically at the second dielectric layer 7.

An embodiment of a process for electrically connecting a drain region of a floating gate, non-volatile memory element to a second metal level, is now described with reference to Figures 3-8. The process uses two dielectric layers, as previously described.

In detail, the manufacturing method starts with conventional steps typical of a MOS process, as far as depositing and planarizing a first insulating layer of dielectric material. In the example shown in Figure 3, a structure is illustrated as having a substrate 25 of P-type and a field oxide region 26. A drain region 27 and a source region 28 of N-type is obtained by selectively introducing doping ion species into the substrate 25. A gate oxide region 29 is arranged on substrate 25, as well as a gate region 30. Conductive polysilicon regions 31a, 31b are formed on field oxide region 26. Lastly, there is a first insulating layer 32, typically of silicon oxide SiO_2, having a thickness of, for example, approximately 500 nm. First insulating layer 32 can optionally be formed in two different steps. For example, depositing TEOS (TetraEthylOrthoSilicate), and/or SOG (Spin On Glass), and/or BPSG (Boron Phosphorous Silicon Glass). Preferably, the first insulating layer 32 is planarized through a reflow step, and then through CMP (chemical mechanical polishing), to guarantee optimum planarization of the surface.

Subsequently, on the first insulating layer 32, which is already planarized, a first stop layer 33 of dielectric material, for example, silicon nitride, is deposited with a thickness of, for example, approximately 50 nm. A contact etching mask is formed on the first insulating layer 32, and contacts are opened through the first stop layer 33 and the first

insulating layer 32, using first an etching solution permitting removal of silicon nitride of the first stop layer 33, and then an etching solution removing silicon oxide of the first insulating layer 32. After removing the contact etching mask, the structure of Figure 4 is obtained, where apertures 34, 35 extend as far as conductive polysilicon regions 31a, 31b, and an aperture 36 extends as far as drain region 27.

Apertures 34, 35, 36 are then filled with a conductive material, such as tungsten after any steps of cleaning and depositing a barrier layer, such as titanium nitride (not shown). For example, a filling layer is deposited, and an etch-back step is carried out, for removing the filling layer above the first stop layer 33. Consequently, the filling material remains only inside apertures 34, 35, 36, forming plugs 37, 38, 39, as shown in Figure 5.

Subsequently, a first metal material layer, for example, aluminum or copper is deposited. The first metal material layer, which forms the first metal level, is then defined to form connection regions according to the design. In particular, three connection regions 40, 41, 42 are shown in Figure 6, where connection region 40 is in electrical contact with plug 37. Intermediate islands, such as 10b shown in Figure 1B, are not formed in this step.

A second insulating layer 45, typically of SiO_2, is then formed, similarly to the first insulating layer 32. The second insulating layer 45 is planarized by reflow and CMP. A second stop layer 46, typically of silicon nitride, is then deposited. Then, using a second mask and double RIE (Reactive Ion Etching) with two different chemicals, apertures 50, 51, 52 and 53 are formed, which pass through the second stop layer 46 and second insulating layer 45. As shown in Figure 7, aperture 50 ends at the connection region 40 of the first metal level, aperture 51 ends at plug 38, aperture 52 ends at plug 39, and aperture 53 ends at connection region 42 of the first metal level.

Subsequently, and similarly to the apertures 34, 35, 36 shown in Figure 4, apertures 50-53 are filled with conductive material, typically tungsten, after any steps for cleaning and depositing a barrier layer, by depositing a filling layer and etching back. Thus,

on completion, plugs 55, 56, 57 and 58 are formed inside apertures 50-53, as shown in Figure 8. In particular, plug 56 is aligned and in direct electrical contact with plug 38, and plug 57 is aligned and in direct electrical contact with plug 39.

A second metal material layer, for example, aluminum or copper, is then deposited and defined to form the second metal level. Three connection regions 60, 61, 62 are then formed, where connection region 60 is in electrical contact with plug 55, connection region 61 is in electrical contact with plug 56, and connection region 62 is in electrical contact with both plug 57 and plug 58. Thereby, connection region 61 is in electrical contact with connection region 31b, and connection region 62 is in electrical contact with drain region 27, without requiring intermediate islands on the first metal level. This allows for, among other things, arranging connection region 41 as shown, whereas forming intermediate islands between plugs 56, 38, and 57, 39, is not possible, or would require greater space between connection regions 61 and 62.

Figure 9 shows a variant of Figure 8, wherein connection regions 40 and 42 of the first metal level are protected from over-etching when forming stacked plugs 56, 57. In fact, as already stated, over-etching, which is necessary to form the plugs 56, 57, in general does not significantly damage the connection regions 40, 42, where the apertures 50, 53 are formed, by virtue of selectivity of metal with respect to connection region etching. However, to minimize damage to the metal in several conditions, it is possible to protect these connection regions, 40, 42 by first depositing the stop layer and then the inter-metallic dielectric layer, which prevents breakdown. This solution is shown in Figure 9, wherein the parts common to Figure 8 have the same reference numbers. In detail, a second stop layer 46a is disposed directly above the first metal level, including connection regions 40-42, and is open only at the plugs 56-58. The second dielectric layer 45a extends above. Consequently, first stop layer 33 is no longer necessary. However, optionally, and similarly to layers 45a, 46a, a silicon nitride stop layer can be arranged below the first dielectric layer 32 of oxide, in a manner not shown in Figure 9.

For manufacturing the device of Figure 9, after the first level connection regions 40-41 have been defined, first the second stop layer 46a, for example, of nitride, and then the second dielectric layer 45a, for example, of oxide, are deposited. Subsequently, the apertures 50-53 are formed by carrying out initial RIE with a first etching chemical, to selectively remove oxide of the second dielectric layer 45a. This step includes an over-etching as necessary in order to excavate the greater depth at the plugs 38, 39, and is stopped automatically at the second stop layer 46a. A second RIE step is then carried out with a second etching chemical, in order to selectively remove nitride of the second stop layer 46a, for a time correlated to the thickness of second stop layer 46a. Thereby, the second connection regions 40, 42 are protected by the second stop layer 46a during over-etching necessary to form plugs 56, 57.

The advantages of the described device and the method are the followings. First, the bulk for connecting connection and/or integrated regions arranged on non-adjacent levels is reduced. In addition, the described method comprises only known process steps and can therefore be implemented using equipments commonly used in the microelectronics industry. The method is simple and reliable, and does not create problems of implementation. If a double dielectric layer is used, as shown in the embodiment of Figures 3-8, it is possible to carry out slight over-etching of the upper dielectric layer, that is the second insulating layer 45. Thus, this ensures that the apertures, that is the apertures 50-53, are formed correctly. Even if the etching masks are misaligned, etching of an upper insulating layer, that is, upper insulating layer 45, stops automatically at the underlying stop layer, that is, the first stop layer 33.

Finally, it is apparent that many modifications and variants can be made to the device and method described and illustrated here, all of which come within the scope of the invention, as defined in the attached claims. In particular, it is emphasized that the described structure can be applied to devices of a different type, as long as they comprise at least two metal levels. In addition, in general, it allows connection between a metal level N-1 and a metal level N+1, thus eliminating the intermediate islands on metal level N. The

described solution can also be replicated on additional, upper metal levels such as to obtain a plurality of apertures and plugs stacked one on another, for as much as 3 or 4 levels. Any method for planarizing the insulating layer can be used, for example may not include CMP. The dielectric stop layer can be provided on only some levels or on none of them, if the manufacturing method used guarantees a high level of alignment of the masks.